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**INFORMATION DISCLOSURE
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Sheet	1	of	1	Application Number	Not Yet Assigned
				Filing Date	Herewith
				First Named Inventor	Juan-Antonio Carballo
				Art Unit	Not Yet Assigned
				Examiner Name	Not Yet Assigned
				Attorney Docket Number	AUS920030890US1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/JT/		KUN JUNG CHANG, ET AL., 50 GB/S 32X32 CMOS Crossbar Chip Using, VLSI Circuits Issue Digest of Technical Papers, 1999, pp. 17-19.	
/JT/		M. J. LEE, ET AL., 84 -m W 4-Gb/s Clock and Data Recovery Circuit for Serial Link Applications, Symp[osium on VLSI Circuits Issue Digest of Technical Papers, 2001, pp. 149-152.	
/JT/		J.M. KHOURY, ET AL., High Speed Serial Transceivers for Data, IEEE Communications Magazine, Issue July 2001, Vol. 39, Issue 7, pp. 160-165.	
/JT/		R. FARJAD-RAD, et al., C. 3-M CMOS 8 Gigabit/S 4-PAM Serial Link, IEEE Journal of Solid State Circuits, Issue May 2000, pp. 757-764.	
/JT/		W. DALLY, ET AL., Transmitter Equal for 4 Gbits/Second Sig., Proc Hot Interconnects Symposium, Issue August 1996, pp. 29-39.	
/JT/		C.K. KEN YANG, ET AL., 0.5 M CMOS 4GB/S Serial Link Transceiver, IEEE Journal of Solid State Circuits, Issue May 1998, pp. 713-722.	

Examiner Signature	/Julia Tu/	Date Considered	03/15/2007
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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